REMARKS

Claims 1, 3, 4, 10, 12, 17, 23, 36, and 41-45 are pending in the present application. Claims 1, 3, 4, 10, 12, 17, 23, and 36 have been allowed. Claims 41-42, 44, and 45 have been rejected under § 102(e) as being anticipated by Dupuis et al., US Patent 6,727,754 (hereinafter "Dupuis"). Claim 43 has been objected to, but would be allowable if rewritten in independent form. New claim 46 has been added.

Information disclosure Statement

An IDS is being submitted subsequent to this Amendment. Applicants hereby request that the Examiner consider the references listed in the IDS.

Applicants would also like to make the Office aware that an initialed copy of the IDS submitted on 2/13/05 has not been received by Applicants. The IDS submitted 2/13/05 is listed in PAIR.

Prior Art Rejections

Claims 41-42, 44, and 45 have been rejected under § 102(e) as being anticipated by Dupuis. The Examiner alleges that PA 3310 of FIG. 33 and transistors M5 and M6 of FIG. 12 can be read as a first power amplifier stage. The Examiner also alleges that PA 3322 of FIG. 33 and transistors M1 and M2 of FIG. 12 can be read as a second power amplifier stage. The Examiner then alleges that the path having amplifier 3326 of Figure 33 can be read as a feedback path.

Independent claim 41 recites a method of reducing noise in a multi-stage power amplifier, including "providing a first power amplifier stage having an inductance coupled to a first switching device," "coupling a second power amplifier stage to the first power amplifier stage, wherein the second power amplifier stage has an inductance coupled to a second switching

device," and "providing a feedback path from the second power amplifier stage to the first power amplifier stage to force the DC levels of the first and second power amplifier stages to be approximately equal, wherein the feedback path is provided by an amplifier."

Dupuis does not teach or suggest the method recited in claim 41. The Examiner has taken elements from separate figures (FIGS. 12 and 33) to argue why claim 41 is anticipated. Even if the amplifier of FIG. 12 of Dupuis were combined with the circuit of FIG. 33, it is likely that the amplifier of FIG. 12 would comprise PA 22310, not a combination of PA 3310 and op-amp 3322. Such a combination does not anticipate claim 41.

For at least these reasons, applicant asserts that claim 41 is allowable over the prior art. Since dependent claim 42 depends from claim 41, it is also believed that this claim is allowable over the prior art.

Independent claim 44 recites a multi-stage power amplifier including "a first power amplifier stage having an inductance coupled to a first switching device," "a second power amplifier stage having an inductance coupled to a second switching device," and "a feedback path coupled between the second and first power amplifier stages so as to make the DC levels of the first and second power amplifier stages to be approximately equal, wherein the feedback path is formed by coupling an amplifier between the second and first power amplifier stages."

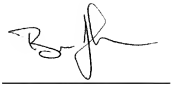
For at least the reasons set forth above with respect to claim 41, applicant asserts that claim 43 is also allowable over the prior art. Since dependent claim 45 depends from claim 44, it is also believed that this claim is allowable over the prior art.

Conclusion

It is respectfully submitted that all claims are patentable over the prior art. It is further more respectfully submitted that all other matters have been addressed and remedied and that the

application is in form for allowance. Should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Bruce A. Johnson, Applicants' Attorney at 512-301-9900 so that such issues may be resolved as expeditiously as possible.

Respectfully Submitted,



3/30/06
Date

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